UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,584	03/09/2006	Toshiharu Takayama	24530-009/MXM	9041

32137 7590 04/27/2009

PATENT DOCKET CLERK
COWAN, LIEBOWITZ & LATMAN, P.C.
1133 AVENUE OF THE AMERICAS
NEW YORK, NY 10036

EXAMINER	
STARK, JARRETT J	

ART UNIT	PAPER NUMBER
2823	

MAIL DATE	DELIVERY MODE
04/27/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,584	TAKAYAMA, TOSHIHARU	
	Examiner	Art Unit	
	JARRETT J. STARK	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6 and 9-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6 and 9-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of group II claims 6, 9, 10 and 11 in the reply filed on 10/8/2008 is acknowledged.

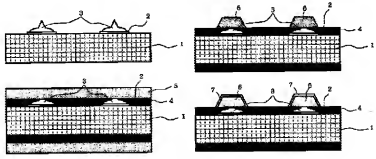
Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naoto (PAJ 2002-033414) in view of Juskey, Jr et al. (US 4,940,181)

【図１】



BASIC-ABSTRACT:
NOVELTY - Metal bump (3) with strap edge for bonding wire, is formed on an aluminum or copper electrode (2) on a semiconductor wafer (1). A copper laminate (5) comprising resin layer is formed over the pressed bump and is

etched to form copper electrode (6) on the bumps. Non-electrolytic nickel plating and gliding (7) is provided to the copper electrode.

Regarding claim 6, Naoto discloses the method for producing a flip-chip mounting electronic component having a plurality of terminals [3]/[2] dotted on a mounting face [1] and a plurality of conductors [6] formed on the terminals, comprising the steps of:

coating the mounting face with a conductor having a predetermined thickness (layer [5]];

masking corresponding positions for the terminal parts on the conductor surface (Abstract); and

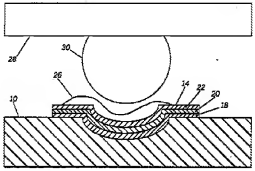
removing the conductor except the mask parts (copper layer [5] is masked and etched to form copper conductor [6]),

the coating, masking and removing steps being carried out in the stated order (see progression of drawings depicted in provided figure 1).

Naoto is however silent upon wherein the conductive material can be coated by electroless plating followed by electrolytic plating. At the time of the invention this claimed coating method was however a well known conventional method for coating conductive materials for analogous device structures. This type of coating process was disclosed by the prior art reference Juskey, Jr et al. Col. 2 lines 52-60 of Juskey disclose:

"*Preferably, the copper layer 18 comprises a first plating of electroless copper having a thickness of 0.05-0.1 mils, topped by a coating of electroplated* [synonymous with electrolytic plating] *copper having a thickness of 1.5-2 mils. For strength and protection, the copper layer 18 is covered with a nickel layer 20 having a preferred*

thickness of 0.15 mils. Finally, the surface of the cavity is coated by a gold layer 22 of approximately 0.04 mils to insure superior electrical connection."



It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Naoto and Juskey to enable the coating step of Naoto to be performed according to the teachings of Juskey because one of ordinary skill in the art at the time of the invention would have been motivated to look to alternative suitable methods of performing the disclosed coating step of Naoto and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP § 2144.07.

Regarding claim 9, Naoto discloses the method for producing a circuit board having a plurality of flip-chip mounting lands dotted on a mounting face (Fig. 1), comprising the steps of:

coating the mounting face with a conductor [5] having a predetermined thickness;

masking corresponding positions for the lands on the conductor surface (Abstract); and

removing the conductor except the mask parts (see progression of layer [5] to conductors [6]), the coating, masking and removing steps being carried out in the stated order (Fig. 1).

Naoto is however silent upon wherein the conductive material can be coated by electroless plating followed by electrolytic plating. At the time of the invention this claimed coating method was however a well known conventional method for coating conductive materials for analogous device structures. This type of coating process was disclosed by the prior art reference Juskey, Jr et al. Juskey discloses:

"Preferably, the copper layer 18 comprises a first plating of electroless copper having a thickness of 0.05-0.1 mils, topped by a coating of electroplated [synonymous with electrolytic plating] *copper having a thickness of 1.5-2 mils. For strength and protection, the copper layer 18 is covered with a nickel layer 20 having a preferred thickness of 0.15 mils. Finally, the surface of the cavity is coated by a gold layer 22 of approximately 0.04 mils to insure superior electrical connection."*

It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Naoto and Juskey to enable the coating step of Naoto to be performed according to the teachings of Juskey because one of ordinary skill in the art at the time of the invention would have been motivated to look to alternative suitable methods of performing the disclosed coating step of Naoto and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP § 2144.07.

Regarding claim 10, Naoto discloses the method for producing a package in which mounting face terminal parts of a flip-chip mounting electronic component and/or flip-chip mounting lands of a circuit board mounting face have conductors (Fig. 1), the method comprising:

forming the conductors as remaining parts from growing formation and/or removal (Fig. 1); and

securing the conductors of the circuit board and the electronic component or the conductors of the electronic component and the circuit board with solder or anisotropic conductive material (Entire document – this limitation is the implicit understood conventional use of the known bump terminal structure).

Naoto is however silent upon wherein the conductive material can be coated by electroless plating followed by electrolytic plating. At the time of the invention this claimed coating method was however a well known conventional method for coating conductive materials for analogous device structures. This type of coating process was disclosed by the prior art reference Juskey, Jr et al. Juskey discloses:

"Preferably, the copper layer 18 comprises a first plating of electroless copper having a thickness of 0.05-0.1 mils, topped by a coating of electroplated [synonymous with electrolytic plating] *copper having a thickness of 1.5-2 mils. For strength and protection, the copper layer 18 is covered with a nickel layer 20 having a preferred thickness of 0.15 mils. Finally, the surface of the cavity is coated by a gold layer 22 of approximately 0.04 mils to insure superior electrical connection."*

It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Naoto and Juskey to enable the coating

step of Naoto to be performed according to the teachings of Juskey because one of ordinary skill in the art at the time of the invention would have been motivated to look to alternative suitable methods of performing the disclosed coating step of Naoto and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP § 2144.07.

Claims 6, 9, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugihara (US 6,406,991 B2) in view of Juskey, Jr et al. (US 4,940,181)

Regarding claims 6, 9 and 10, Sugihara discloses the method for producing a package in which mounting face terminal parts of a flip-chip mounting electronic component and/or flip-chip mounting lands of a circuit board mounting face have conductors (Figs. 5A-G), the method comprising:

forming the conductors as remaining parts from growing formation and/or removal (Figs. 5A-G); and

securing the conductors of the circuit board and the electronic component or the conductors of the electronic component and the circuit board with solder or anisotropic conductive material (Col. 23&24 – this limitation is the implicit understood conventional use of the device).

Sugihara Naoto is however silent upon wherein the conductive material can be coated by electroless plating followed by electrolytic plating. At the time of the invention this claimed coating method was however a well known conventional method for coating conductive materials for analogous device structures. This type of coating process was disclosed by the prior art reference Juskey, Jr et al. Juskey discloses:

"*Preferably, the copper layer 18 comprises a first plating of electroless copper having a thickness of 0.05-0.1 mils, topped by a coating of electroplated* [synonymous with electrolytic plating] *copper having a thickness of 1.5-2 mils. For strength and protection, the copper layer 18 is covered with a nickel layer 20 having a preferred thickness of 0.15 mils. Finally, the surface of the cavity is coated by a gold layer 22 of approximately 0.04 mils to insure superior electrical connection.*"

It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Sugihara and Juskey to enable the coating step of Sugihara to be performed according to the teachings of Juskey because one of ordinary skill in the art at the time of the invention would have been motivated to look to alternative suitable methods of performing the disclosed coating step of Sugihara and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP § 2144.07.

Regarding claim 11, Naoto discloses the method for producing a package according to claim 10, wherein the conductors are constituted of copper and on surfaces thereof a nickel layer and a gold layer are formed in the stated order (Figs. 5A-G), and securing step is carried out by fixing force of solder (Col. 23&24).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JARRETT J. STARK whose telephone number is (571)272-6005. The examiner can normally be reached on Monday - Thursday 7:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michelle Estrada/
Primary Examiner, Art Unit 2823

4/22/2009
/J. J. S./
Examiner, Art Unit 2823